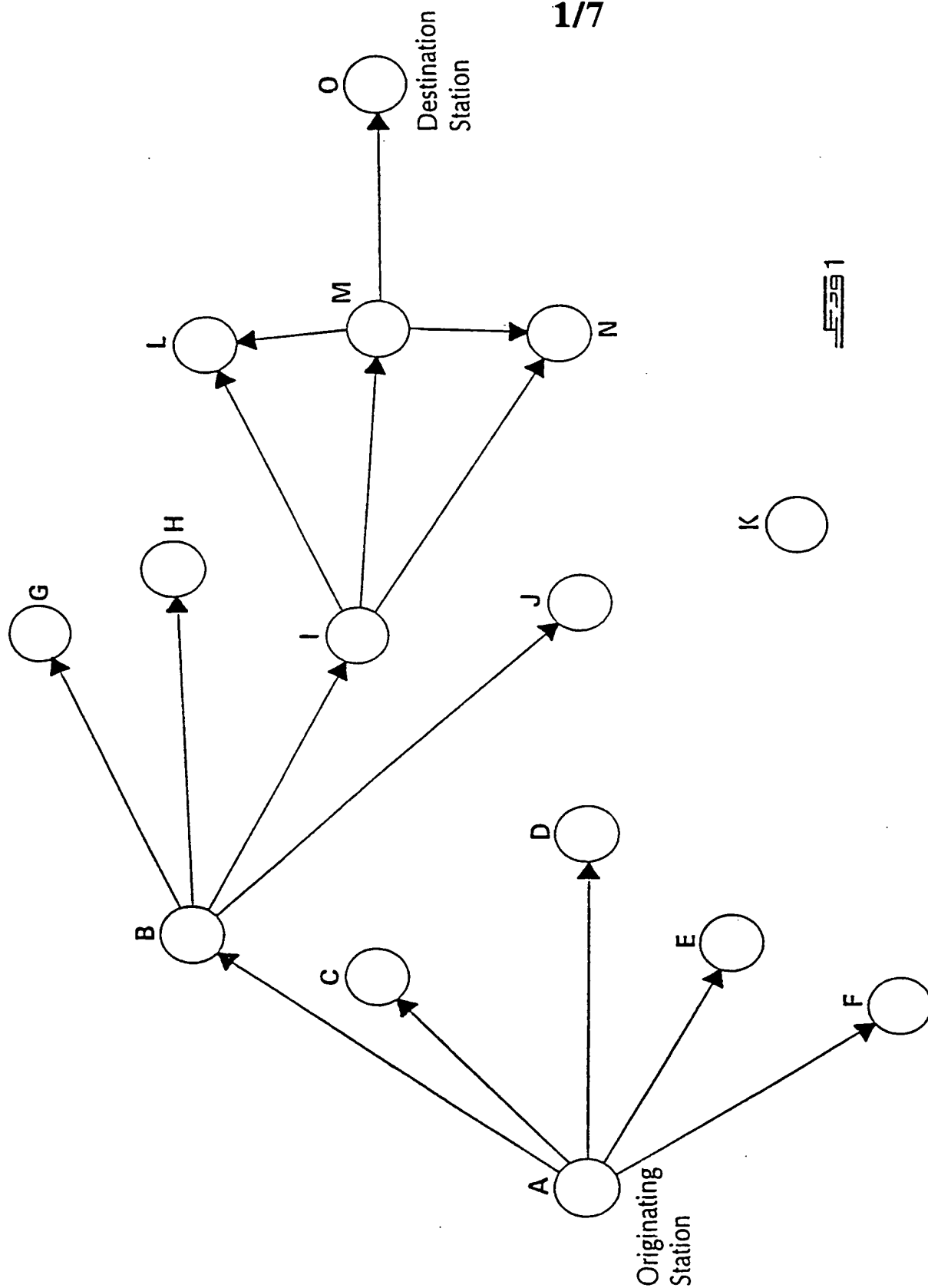
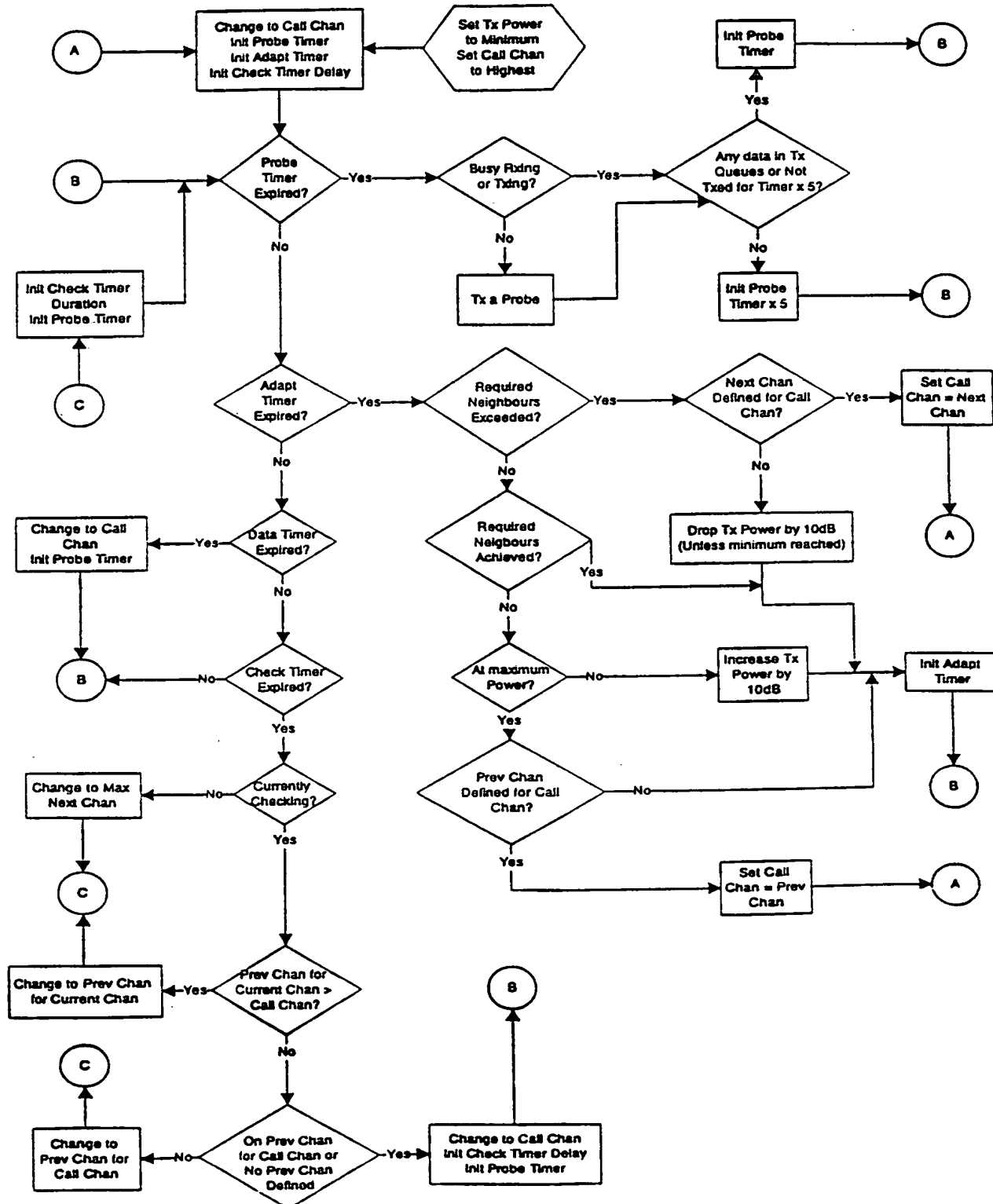


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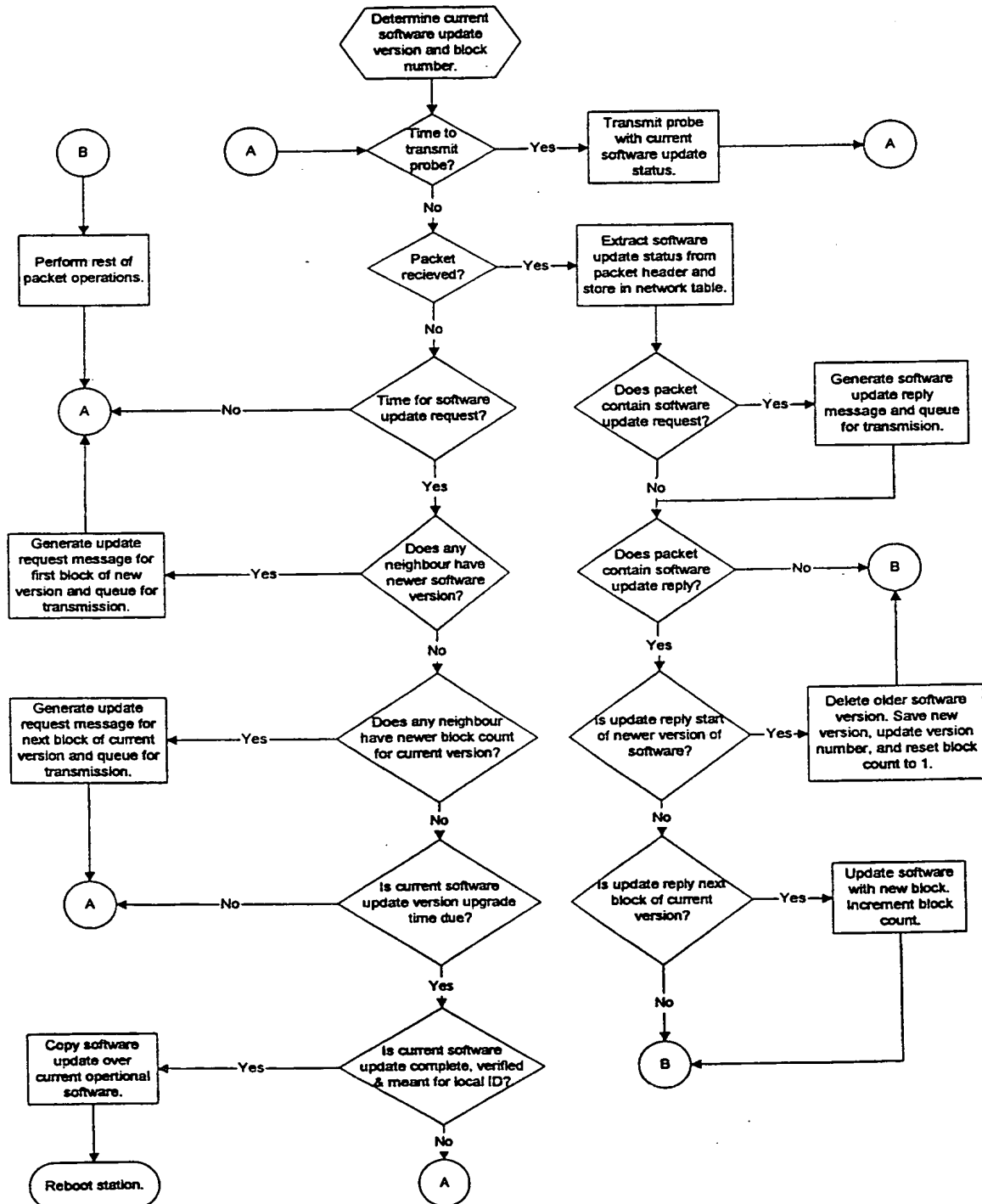
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SSG 3



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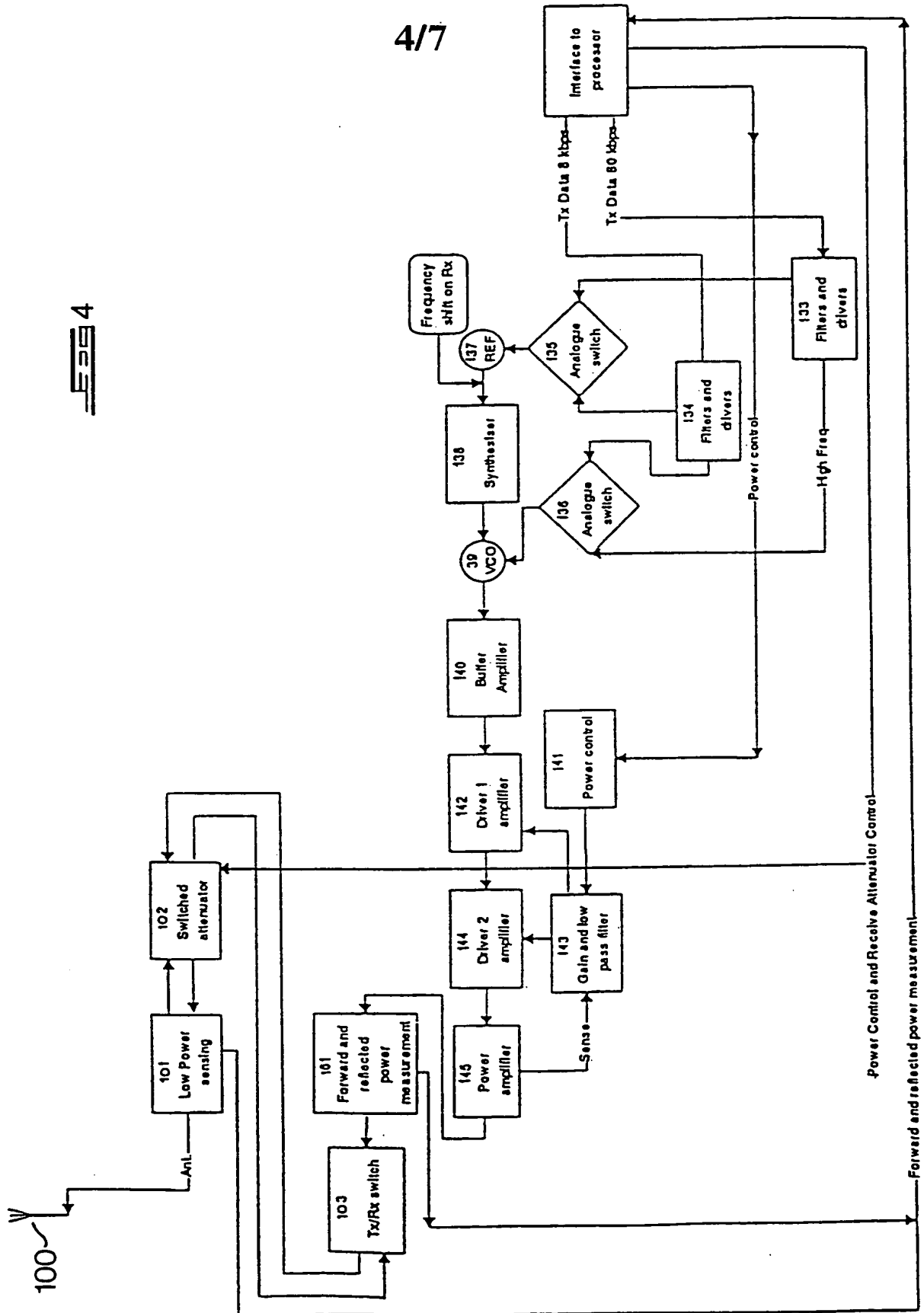




Figure 6 is a block diagram of a communication system architecture. The system includes a Main Processor 386 EX (149) connected to Static and dynamic RAM (150) and a Real time clock (148). The processor is also connected to an Analogue to digital converter (146) and a Peripheral Interface (147). The Analogue to digital converter is connected to an Interface to receiver (207) and a Zilog high speed dual channel synchronous serial chip (131). The Interface to receiver (207) receives Rx Data (00 Kbps) and Rx Data (0 Kbps) and outputs Broad band RSSI, Narrow band RSSI, and Spike count and level. The Zilog chip (131) is connected to a 60 Kbps QMSK FX 509 Modem (129) and a 9 Kbps QMSK FX 509 Modem (127). The 60 Kbps modem (129) is connected to a PN sequence encoding and decoding block (130) and a Power control and receive attenuator control block (132). The 9 Kbps modem (127) is connected to a PN sequence encoding and decoding block (128) and a Power control and receive attenuator control block (132). The Power control and receive attenuator control block (132) is connected to a Transmitter Interface (206) and a Transmitt Data rate switch. The Transmitter Interface (206) is connected to the 9 Kbps modem (127) and the Transmitt Data rate switch. The Transmitt Data rate switch is connected to the Power control and receive attenuator control block (132) and the Transmitter Interface (206). The system is also connected to a Transmitt Data rate switch (132) and a Transmitter Interface (206).

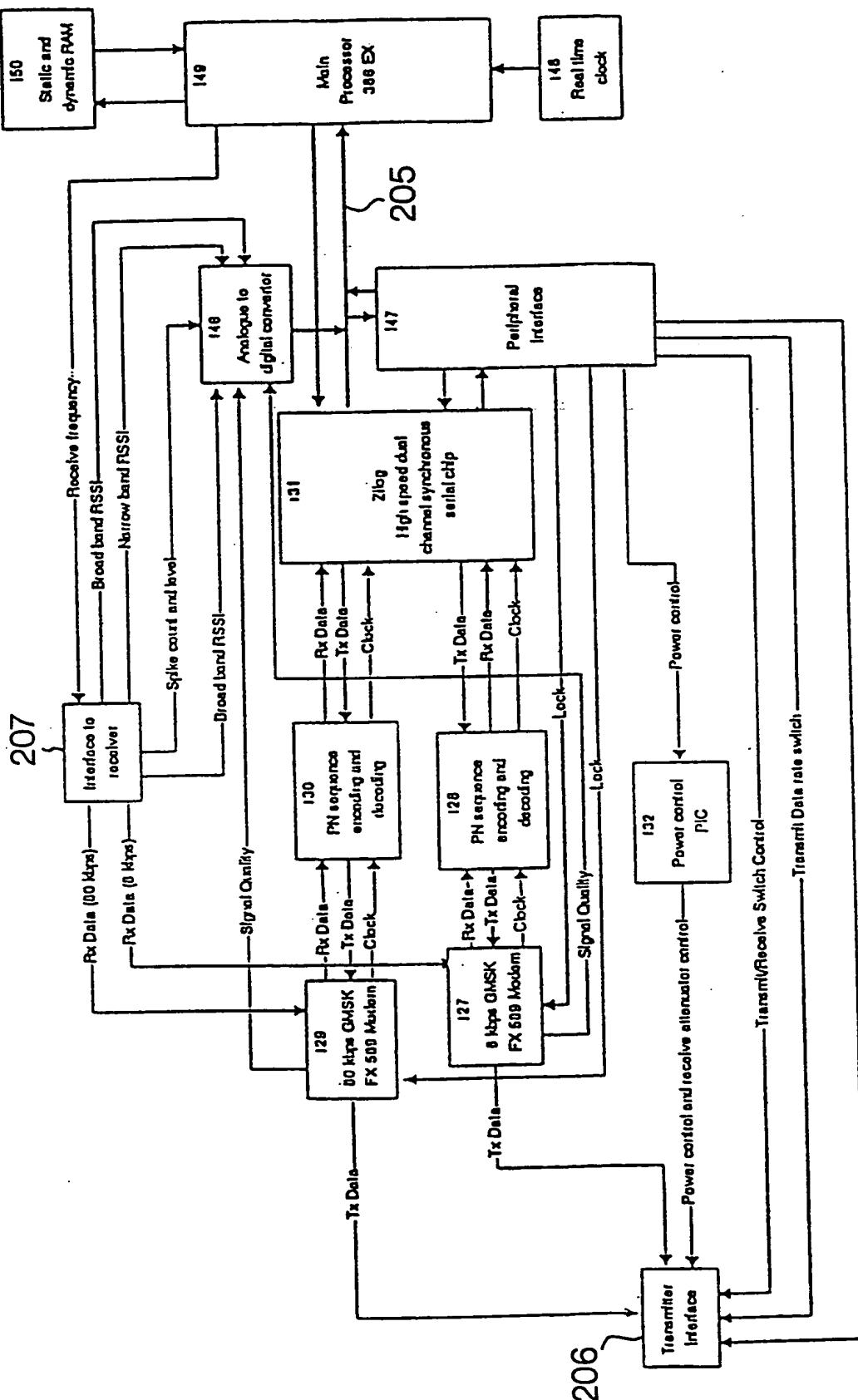


Fig 7